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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,012	11/13/2001	Kenichi Watanabe	011264	6363

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,012	WATANABE, KENICHI	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) *2 - 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 21 - 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on August 6, 2004 has been received and entered in the case.

Election/Restrictions

2. Claims 2 - 20 continue to be withdrawn from consideration for the reasons provided in the Office action mailed on August 1, 2003.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1 and 21 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Iguchi et al. '782.

Regarding claim 1, Iguchi et al. discloses in e.g., Figs. 6 and 19A – 19C a semiconductor wafer device comprising:

- a semiconductor wafer (1 in Fig. 17C; column 1, lines 29) comprising a circuit area (at the circuit layers in Fig. 6) disposed in a central area of said semiconductor wafer and a peripheral area (at the multi-layers in Fig. 19C) disposed around said circuit area of said semiconductor wafer;
- a number of semiconductor elements (transistors on the area 40; column 10, lines 8 – 30) formed on said circuit area;
- a circuit multi-layer wiring structure (the elements 43 and 44 in each layer 45) formed on said circuit area and comprising multi-layer wirings connected to said semiconductor elements and interlevel insulating films (at the each one of the layer 45), at least some of said multi-layer wirings being damascene wirings (column 10, lines 35 – 37) including wiring patterns (44) and via conductors (43) embedded in respective ones of said interlevel insulating films; and
- a peripheral multi-layer structure (at the multi-layers in Fig. 19C) formed on said peripheral area, comprising insulating films (3, 15 and 4; see Fig. 15G) made of extensions of said interlevel insulating films (column 10, lines 22 – 25) and having one or more trenches (at the place where the copper film 6 is filled in; see Fig. 17C and column 11, line 5) formed in respective one or ones of said insulating films, each of said trenches having opposing sidewalls and a bottom surface in associated one of said insulating films (3, 15 and 4), and a conductor pattern (6; copper) filling etch of said trenches and made of a same material (see Fig. 19A) as said wiring patterns (copper 44; Fig. 6 and column 10, line 16) in associated one of said interlevel

insulating films and not having conductor patterns corresponding to said via conductors.

Regarding claim 21, Iguchi et al. discloses in e.g., Figs. 6, 15G and 19A – 19C a semiconductor wafer device, comprising:

- an underlying structure (1) including a semiconductor wafer;
- a first insulating layer (HSQ layer 15, k = 2.8 through 3.2; column 10, lines 1 – 7 and Fig. 15G) having a lower dielectric constant than silicon oxide (k = 3.9 through 4.2) and formed over said underlying structure in an area excepting a peripheral area of said underlying structure;
- a second insulating layer (silicon oxide film 4; column 10, line 43) having a dielectric constant higher than said first insulating layer and formed on said first insulating layer;
- grooves (at the opening areas between the element 15) formed at least through said second insulating layer;
- patterns of conductor filled (6; Fig. 19C) in said grooves;
- said second insulating layer or a layer (copper film 6 in Fig. 19C) of a same material as the conductor covering an outermost side wall of said first insulating layer, and wherein
- a multi-layer peripheral structure (3 and 4) is formed on said peripheral area not formed with circuits, comprising one or more of said grooves and conductor patterns filling said grooves (copper film 6).

Regarding claim 22, Iguchi et al. discloses in e.g., Figs. 6, 15G and 19A – 19C said interlevel insulating films (3, 15 and 4) including a first insulating layer (HSQ layer 15, k = 2.8 through 3.2; column 10, lines 1 – 7 and Fig. 15G) having a lower dielectric constant than silicon oxide (k = 3.9 through 4.2) and formed over said semiconductor wafer (1) in an area except said peripheral area, and a second insulating layer (silicon oxide film 4; column 10, line 43) having a dielectric constant higher than said first insulating layer and formed on said first insulating layer and said device further comprising said second insulating layer or a layer (copper film 6 in Fig. 19C) of a same material as the conductor covering an outermost side wall of said first insulating layer.

Regarding claim 23, Iguchi et al. discloses in e.g., Figs. 6, 15G and 19A – 19C A semiconductor wafer device comprising:

- a semiconductor wafer (1 in Fig. 17C; column 1, lines 29) comprising a circuit area (at the circuit layers in Fig. 6) disposed in a central area of said semiconductor wafer and a peripheral area (at the multi-layers in Fig. 19C) of said semiconductor wafer not formed with circuits;
- a number of semiconductor elements (transistors on the area 40; column 10, lines 8 – 30) formed in said circuit area;
- a circuit multi-layer wiring structure (the elements 43 and 44 in each layer 45) formed on said circuit area and comprising multi-layer wirings connected to said semiconductor elements and interlevel insulating films (at the each one of the layer 45), said interlevel insulating films comprising a first interlevel insulating film having a wiring trench (at the place of the element 44) formed from an upper surface to an

intermediate depth of said first interlevel insulating film, and a via hole (43) formed from a bottom surface of said wiring trench to a bottom surface of said first interlevel insulating film, said multi-layer wirings including a damascene wiring (column 10, lines 35 – 37) including a wiring pattern filling said wiring trench, and a via conductor filling said via hole; and

- a peripheral multi-layer structure (at the multi-layers in Fig. 19C) formed in said peripheral area, comprising insulating films (3, 15 and 4; see Fig. 15G) made of extensions of said interlevel insulating films (column 10, lines 22 – 25), including a first insulating film made of an extension of said first interlevel insulating film and having one or more trenches (at the place where the copper film 6 is filled in; see Fig. 17C and column 11, line 5) formed from an upper surface to an intermediate depth of said first insulating film, said peripheral multi-layer structure including a conductor pattern (copper 6) or patterns filling said one or more trenches and made of a same material (see Fig. 19A) as said wiring (copper 44; Fig. 6 and column 10, line 16) in the same layer and not having conductor patterns corresponding to said via conductor.

Response to Arguments

5. Applicant's arguments with respect to claims 1 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more

information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Monday, October 25, 2004

GEORGE ECKERT
PRIMARY EXAMINER